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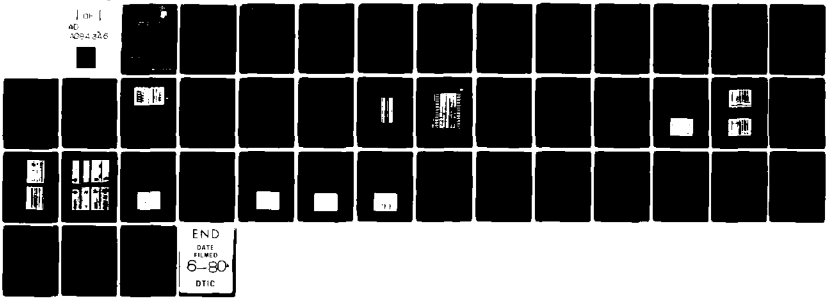

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RADC-TR-79-331
Final Technical Report
February 1980

ANALOG-BINARY PROGRAMMABLE TRANSVERSAL FILTER

RCA Advanced Technology Laboratories

J. R. Tower
L. D. Elliott
D. A. Gandolfo

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APPROVED: Lyn H Skolnik

LYN H. SKOLNIK
Project Engineer

APPROVED: Robert M Barrett

ROBERT M. BARRETT, Director
Solid State Sciences Division

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This Final Technical Report on the Analog-Binary Programmable Transversal Filter program emphasizes the testing of the TC1235 CCD correlator device. The Interim Technical Report for this program contained a statement of the objectives, a general description of the analog-binary correlator, and a detailed design description of the correlator device. For convenience, a portion of the Introduction and Summary section of that report is reproduced here.

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The objective of this program was to develop a programmable CCD (Charge-Coupled Device) circuit capable of correlating a variety of binary-coded waveforms. This analog-binary correlator stores a binary waveform as a reference, and then compares newly arriving signals to the reference waveform. In general, the signal is a binary code that has been corrupted in the transmission channel so that upon arrival at the receiver, it really has an analog character (i.e., the amplitude varies continuously). Analog-binary correlation techniques have an important advantage over purely digital approaches. If the analog signal is directly compared to the reference, only a single correlation channel is required, whereas a digital correlator requires a separate channel for each bit of resolution in the analog-to-digital converter. Thus, a reduction in parts count, with attendant improvements in size, cost and reliability, is realized with the CCD correlator.

The correlator is an important device because correlation of binary waveforms is a function widely used in spread spectrum systems, which offer important advantages for military communications and radar applications. Spread spectrum advantages include jam resistance, reduced detectability and improved signal-to-noise ratio for given transmitter power. Thus, the device whose design is described here should be broadly useful in military systems.

Specified and expected performance of the analog-binary programmable transversal filter device are summarized below:

Performance Parameter	Contract Requirement	RCA Design Goal
Number of Points Correlated	512	512, 256, 126, 64
CCD Clock Rate	8 MHz	10 MHz
Reference Code Load Rate (Program Register)	0.5 MHz	5 MHz
Dynamic Range (Single Tap)	35 dB	45 dB
Signal-to-Noise Ratio (Single Tap)	50 dB	66 dB
Charge Transfer Inefficiency ($n\epsilon$)	0.2	0.1

A further objective of the program was to simplify the interface between the CCD correlator and the surrounding system by including many support circuits on the CCD chip. Support circuits include clock drivers, reference code load logic, and TTL-MOS level translators.

The Interim Technical Report (January 1979) includes a general description of the analog-binary programmable transversal filter device, designated TC1235 (Section 2) and a detailed discussion of the design of all the circuits on the chip (Section 3). Section 2 includes: a brief description of earlier devices, the manner in which the CCD correlator operates, correlator interfaces with off-chip circuits, and timing information. Section 3 includes: a description of the buried channel CCD/NMOS process with self-aligned diffusions, and detailed circuit designs. Particular attention is given to major features which were not included in earlier correlator designs. These are the tap structure, uniphase clocking, and a corner-turning circuit. The tap structure is believed to be highly significant in that it eliminates the code-dependent bias problem. In earlier correlator designs, the correlation signal is superimposed on a bias current which is independent of the signal, and which depends on the number of ones and zeroes in the code. As a result, the bias signal changes when the code is changed. This problem surfaced early in the design study phase of the program, and considerable subsequent effort was expended working out a design that was first proposed by the MIT Lincoln Laboratory. With this tap circuit, the new correlator will not be limited to balanced codes, i.e., codes containing equal numbers of ones and zeroes.

In this Final Technical Report, Section 2 (Test Module) discusses the tester circuitry with emphasis on two of the most important off-chip circuits: the CCD transport clock buffer and the summing circuits. Section 3 (Device Test Results) provides the correlation data, including near-theoretical autocorrelation response (peak-to-side-lobe ratio = 25.4 dB out of a possible 26.5 dB), and data for each of the sections of the device. Section 4 (Conclusions and Recommendations) highlights the most important findings and suggests areas where further effort may be fruitful.

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PREFACE

The work discussed in this document was performed under Air Force Contract F19628-77-C-0263, Analog-Binary Programmable Transversal Filter. This is the Final Technical Report (CDRL Sequence Number 105, Line Item 0002) covering the period from 9/30/77 through 6/30/79. RCA Government Systems Division, Advanced Technology Laboratories in Camden, NJ, is the organization responsible for the work. Dr. D.A. Gandolfo was the principal investigator. The work was monitored by Dr. F.D. Shepherd and Dr. L.H. Skolnik, Electronic Systems Division, Deputy for Electronics Technology, Hanscom AFB, MA.

The report was prepared by J. R. Tower, L.D. Elliott, D. A. Gandolfo. The following RCA personnel contributed to the work discussed: J. R. Tower, B. M. McCarthy, L. D. Elliott, J. I. Pridgen, D. A. Gandolfo (Advanced Technology Laboratories); R. Angle, D. Sauer, F. Shallcross (RCA Laboratories, Princeton). A valuable contribution (a new tap structure design) was made by S. C. Munroe of the MIT Lincoln Laboratory.

EVALUATION

1. This report is the Final Report on the contract. It covers development of a CCD based analog-binary programmable transversal filter during the period 30 Sep 77 to 30 Jun 79. The objective of the research is the generation of a versatile, programmable correlator and experimental verification as to its ultimate usefulness for signal processing applications. The resultant device represents a significant improvement over previous CCD correlator technology in that code dependence bias problem has been eliminated. Operation at a 10 MHz rate makes this chip attractive for incorporation in future spread spectrum systems.

2. The above work is significant since it demonstrates a new technology which makes possible improved devices for accomplishing real time signal processing tasks in communications, USAF, and ECM systems.

LYN H. SKOLNIK
Project Engineer

Section I

INTRODUCTION

This Final Technical Report on the Analog-Binary Programmable Transversal Filter program emphasizes the testing of the TC1235 CCD correlator device. The Interim Technical Report for this program contained a statement of the program objectives, a general description of the analog-binary correlator, and a detailed design description of the correlator device. For convenience, a portion of the Introduction and Summary section of that report is reproduced here.

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In this Final Technical Report, Section 2 (Test Module) discusses the tester circuitry with emphasis on two of the most important off-chip circuits: the CCD transport clock buffer and the summing circuits. Section 3 (Device Test Results) provides the correlation data, including near-theoretical autocorrelation response (peak-to-side-lobe ratio = 25.4 dB out of a possible 26.5 dB), and data for each of the sections of the device. Section 4 (Conclusions and Recommendations) highlights the most important findings and suggests areas where further effort may be fruitful.

Section 2.0

TEST MODULE

2.1 TEST MODULE DESCRIPTION

The Test Module permits preliminary evaluation of the RCA TC1235 Analog/Binary Correlator independent of specific system constraints and with a minimum requirement for external support equipment. The required input sources are a +28Vdc power supply with a 2 A minimum current capability, a -28Vdc power supply with a 500 mA minimum current capability, and ground. Also required is a generator that can provide a 20 MHz square wave into 50 ohms at T^2L levels. The outputs provided are an oscilloscope trigger and the correlation signal, both to be terminated into 50 ohms.

A system block diagram is given in Fig. 2-1. The following description gives the functional details of the five system boards that comprise the Test Module.

2.1.1 Correlator Board

This board contains the TC1235 socket, the transport clock driver (ϕ_T) buffer circuit, the Σ line to the Difference Signal Processing Board impedance buffers, dc

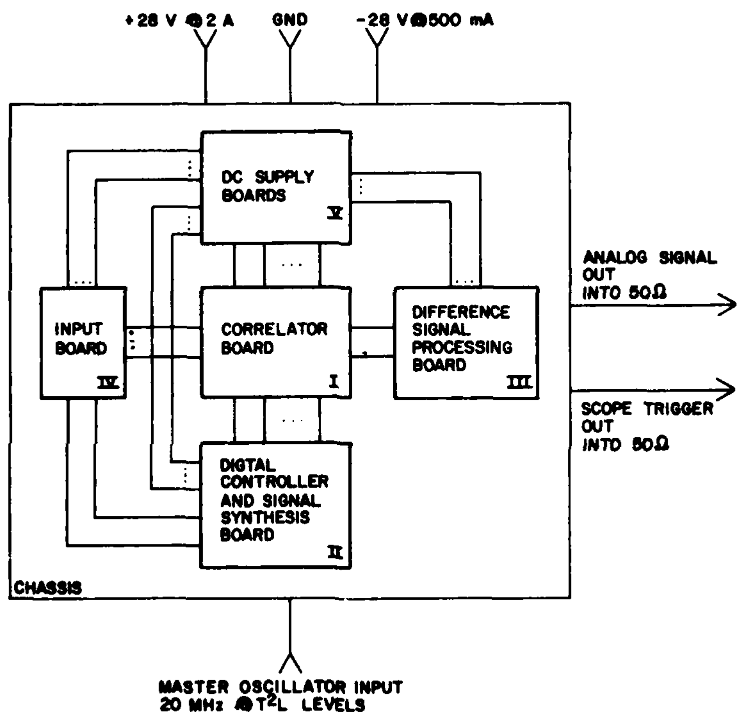


Figure 2-1. TC1235 Test Module block diagram.

isolation and bypassing components, clamping circuits, digital-signal line termination components, digital-level translation circuits, a level adjustment for the signal to the Analog Input port of the TC1235, and signal monitoring test points.

2.1.2 Digital Controller and Signal Synthesis Board

This board contains the system timing and control circuits, a signal synthesis circuit that provides nine different switch-selectable functions, and a variable-duty-cycle gating circuit. The signal synthesis circuit will generate two aperiodic maximal-length sequences, two non-optimal-length aperiodic sequences, three different square waves, a one-chip-wide pulse, and a constant no-signal condition. The variable gating circuit is switch activated to allow truncated or periodic operation of the binary codes at the generator. When switched to any of the square waves, however, only the signals at the Analog Input port of the TC1235 will be selectively truncated. In addition to the above circuits, two switches are provided to control data loading of the on-chip latches of the TC1235.

2.1.3 Difference Signal Processing Board

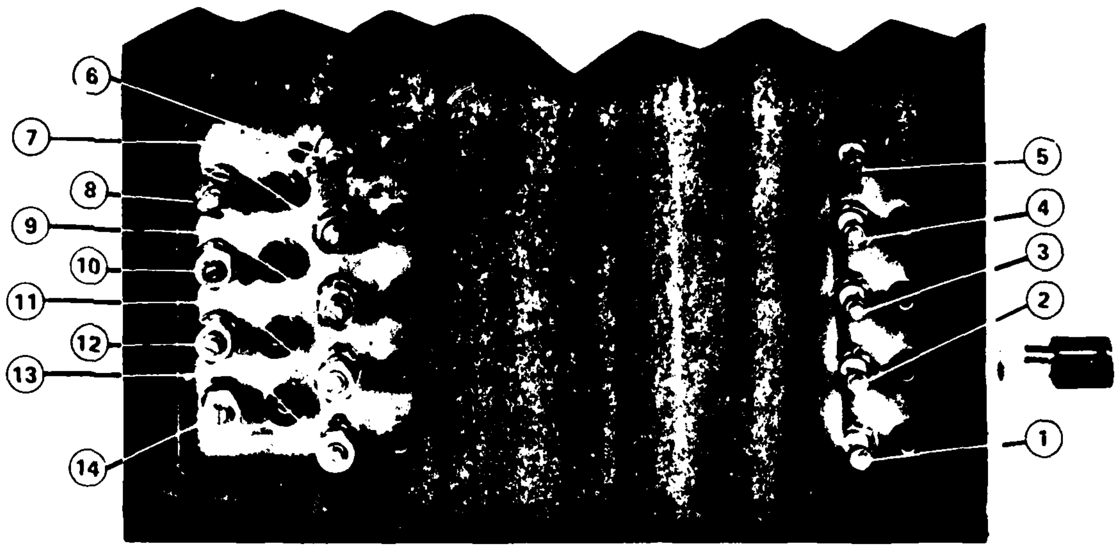
To extract the correlation signal, the difference outputs of the TC1235 must be externally summed; this board performs this function. In addition to a differential amplifier, the board contains two 50-ohm, five-section Butterworth filters; an impedance buffer; one 50-ohm, seven-section Butterworth filter; and an externally accessible, adjustable, 50-ohm attenuator.

2.1.4 Input Board

This board performs the function of converting the selected binary signal (generated by the Signal Synthesis circuits) to a continuously variable, three-level signal. In performing this operation, an automatic gating action is also obtained when switched to a square-wave signal. An externally accessible adjustment is provided to permit independent variation of the dc level of the no-signal interval of the gated waveform.

2.1.5 DC Supply Boards

These circuits comprise two boards in the system and several chassis-mounted components. The circuits provide all of the voltages needed on-chip to operate the TC 1235, in addition to the operating voltages for all of the system circuits. As shown in Fig. 2-2, there are five primary and nine secondary adjustments, which can be externally accessed to allow optimal device parameter adjustment. Monitoring test points have been provided for each of these voltages. As an added precaution, input-voltage, reverse-polarity protection circuits have also been incorporated. A front-panel-mounted, lighted on-off switch is provided for convenience.



(1) G_1: Clamp level adjustment, active during the signal interval of the aperiodic input to the Analog Signal Input port of the TC1235.

(2)(3) G_2 & G_3: Variable dc to the input structure dc gates of the CCD.

(4) ΣV_{GG}: Variable dc to the gates of the tap FET active loads.

(5) ϕ_{DCFG}: Variable dc to the dc gates just prior to the floating gates in the CCD register.

(6) $\phi_{DC\ output}$: Variable dc to the dc isolation gate located between the floating diffusion and the reset gate in the output circuit of the CCD.

(7) ϕ_{RG}: Clamp level adjustment for the reset pulse of the CCD.

(8) V_{GGFF}: Variable dc to the gates of the latches.

(9) Sub: Variable dc to the substrate.

(10) ΣV_{DD}: Variable dc to the drains of the tap buffer FETs.

(11) ϕ_T amplitude: Variable dc to the T buffer circuit to adjust the amplitude of the transport clock.

(12) ϕ_{FGR}: Clamp level adjustment for the floating gate reset pulse applied to the gate of the floating gate reset transistor.

(13) ϕ_T: Clamp level adjustment for the transport clock.

(14) V_{BIAS}: Variable dc to the drain of the floating gate reset transistor.

Figure 2-2. Test Module adjustment locations.

2.2 ϕ_T BUFFER

A buffer-driver is required to boost the drive capability of the on-chip CCD transport driver. The driver must accept the transport driver output (ϕ_T') and produce the transport clock ϕ_T. The output from the on-chip transport driver is a clock of amplitude V_{DD}, which can drive a 130-pF load (V_{DD} = 10V). The buffer must accept this clock and produce a clock of 17V nominal amplitude (16V to 18V range). The load on the output of the buffer is approximately 240 pF; this is the capacitance of the CCD transport gates (ϕ_T gates plus package capacitance).

The first version of the ϕ_T buffer is shown in Fig. 2-3. This bipolar buffer is easy to implement and gives fairly good results. A better version of the buffer is given in Fig. 2-4. This circuit exhibits rise and fall times of 12 ns when driving the TC1235 ϕ_T load.

2.3 SUMMING CIRCUIT

The correlator requires an off-chip post-processing operation of differential summation of the voltage signals on the summation buses (Σ^+ and Σ^-). The most attractive method for attaining the summation is to employ a single differential amplifier with high common-mode rejection. A good candidate for the differential amplifier is the National LM733 video amplifier.

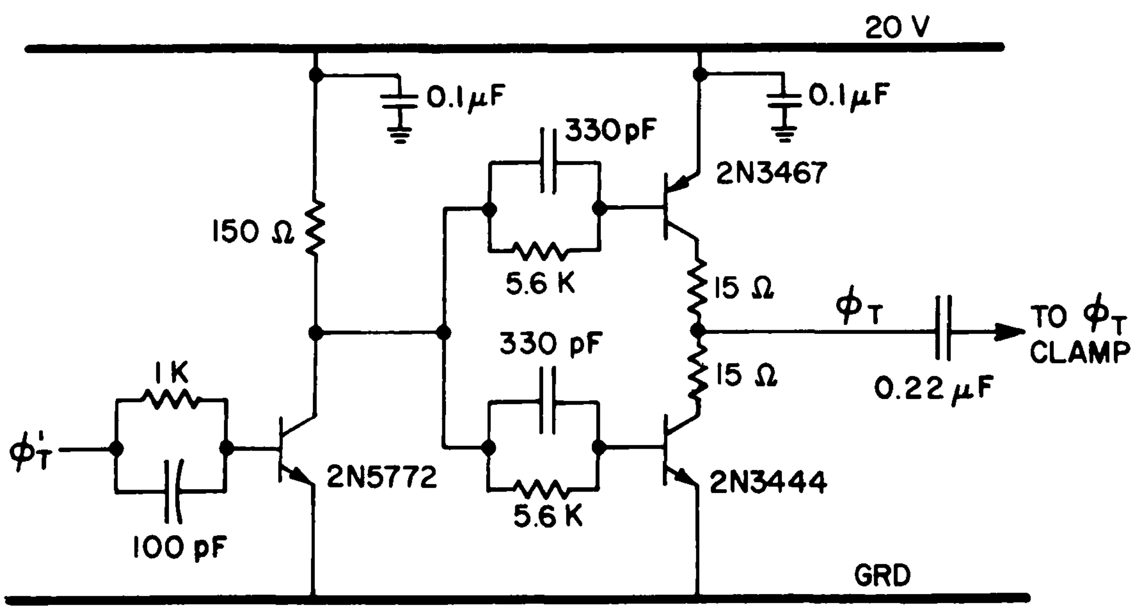


Figure 2-3. Bipolar transport clock buffer.

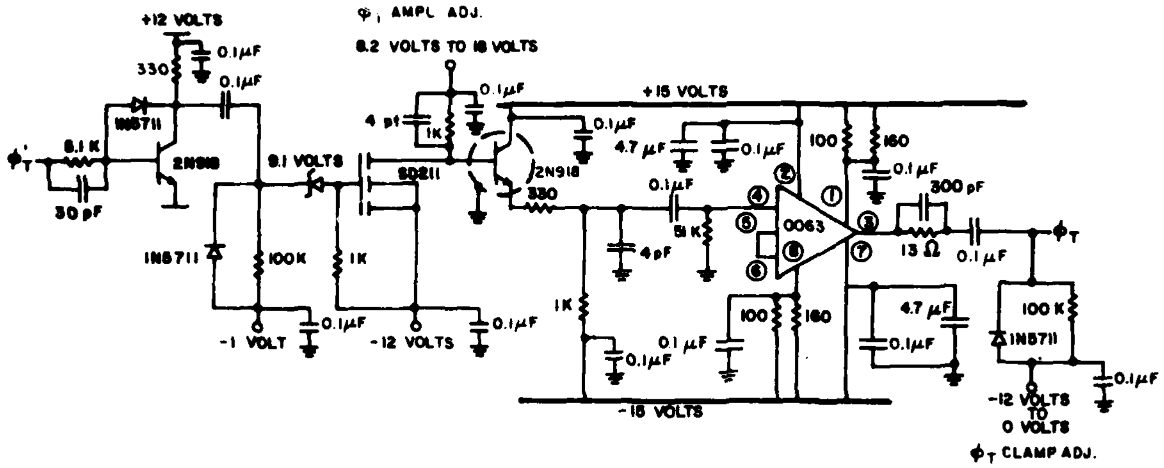


Figure 2-4. Preferred ϕ_T buffer

There is considerable clock feedthrough present on the summation buses; for this reason, the tester employs a summation circuit that utilizes low-pass filtering. The circuit employed for the tester and for all the results presented in this report is given in a block diagram form in Fig. 2-5. The buffers (A) are National LH0002 current buffers. The first low pass filters (B) are 20-MHz, five-section Butterworth filters. The summation amplifier (C) is the National LM733 video amplifier. The output low pass filter is a 15-MHz, seven-section Butterworth filter (D).

2.4 DEVICE PACKAGING

The TC1235 chips are packaged in a Kyocera 64-pin, dual-in-line, ceramic package. The square cavity of the package is 400 mils (±8 mils) on an edge. The die attach pad is gold plated and is connected to pin 16 (key pin numbers are printed on the package). The majority of the dice are mounted to the die attach pad with a silver, electrically conductive epoxy.

The cavity is sealed by a lead-Kovar lid, which has a tin preform attached. The lids are supplied taped on. The tin preform may be employed to hermetically seal the

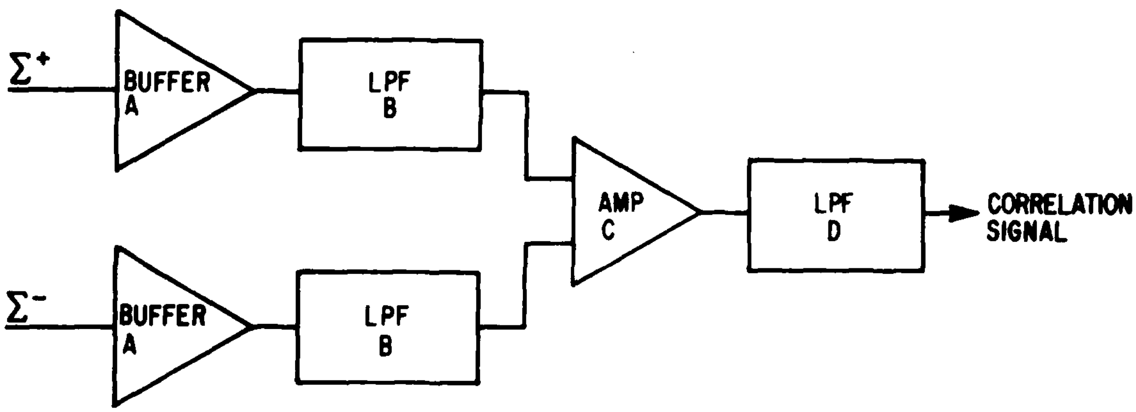


Figure 2-5. Summing circuit block diagram.

cavity by applying appropriate heating. The leads of the package are bent toward the lid in order to allow a heat sink to be placed on the back side of the package.

A bonding diagram is shown in Fig. 2-6. A photograph of a packaged device is given in Fig. 2-7. Table 2-1 lists the pin connections for the device.

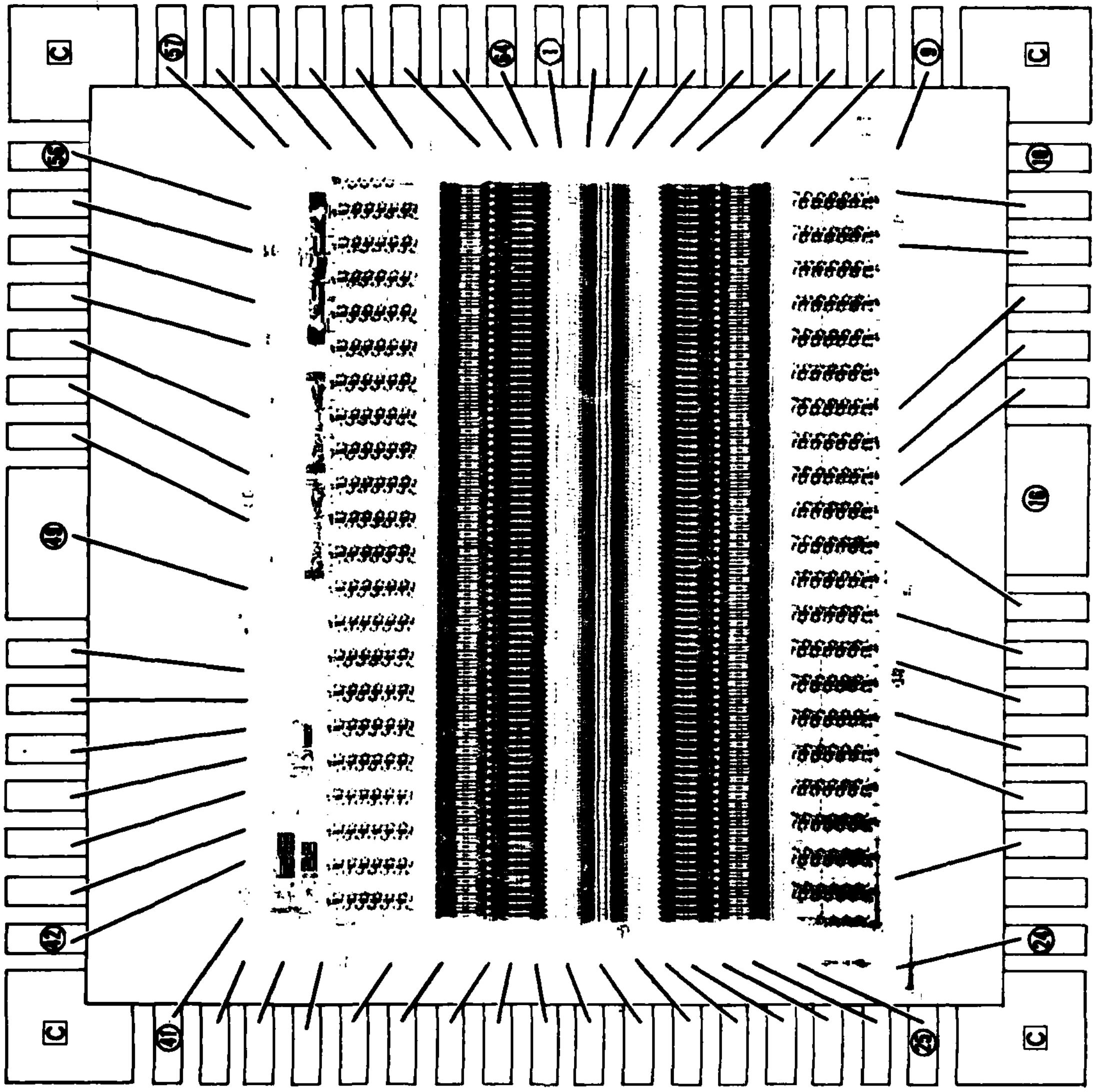


Figure 2-6. Bonding diagram for TC 1235.

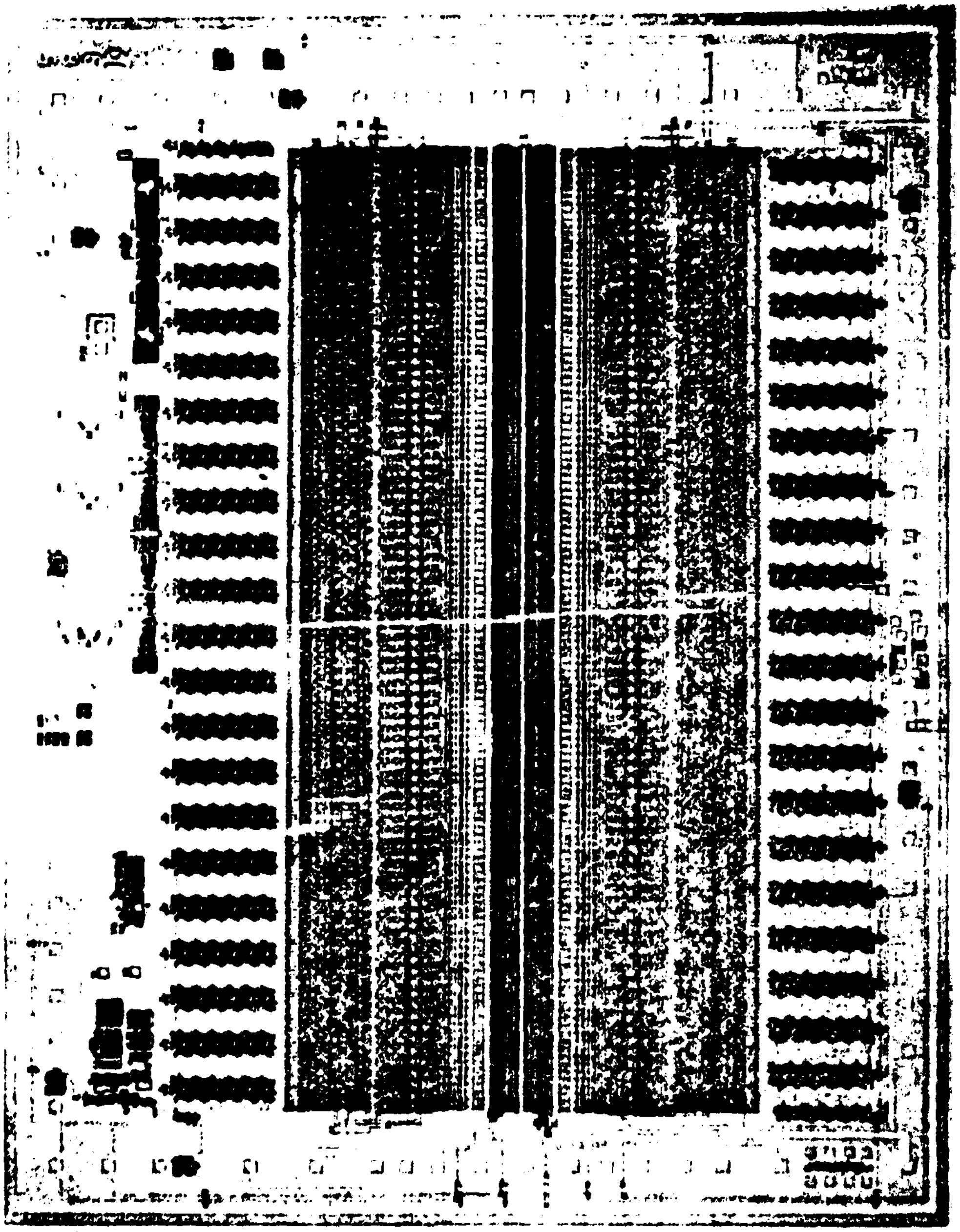


Figure 2-7. Photomicrograph of TC 1235.

TABLE 2-1. TC1235 I/O PADS

Pad Designation	Typ. Voltage
1. ΣV_{SS} GRD; Source of Tap FET Active Load	GRD
2. ϕ_{DCFG} dc Gate; Just Before Floating Gate in CCD Reg.	1.4
3. V_{BIAS} Drain of FGR Transistor, Drain of CCD Out. Trans.	2.6
4. ΣV_{DD} Drain of Tap FET	10.7
5. $\Sigma^{(-)}$ One End of Buss (Bottom Right of Chip)	
6. $\Sigma^{(+)}$ One End of Buss (Bottom Right of (Chip)	
7. V_{SSFF} Source Rail of Latches (GRD)	GRD
8. V_{DDFF3} 3rd Bank of Latch Drains	10
9. V_{DDFF4} 4th Bank of Latch Drains	10
10. N/C	
11. ϕ_{RESET} Latch Reset Input to Bottom 1/2	9 V Swing
12. PR_{in2} Data Input to Bottom 1/2	9 V Swing
13. ϕ_B Buss Input Bottom 1/2	8 V Swing
14. ϕ_A Buss Input Bottom 1/2	8 V Swing
15. V_{DDPRG} Drain Volt. for Bottom 1/2	10
16. N/C	
17. GRD	GRD
18. SUB	-0.8
19. $\phi_{DC(output)}$ dc Isolation Gate after out. F.D. (Between F.D. and Reset Gate)	15
20. $V_{DD(output)}$ Drain of First Stage of CCD Output Amp.	15
21. PR_{out2} Output of Bottom Half	8 V Swing
22. ϕ_{ISO} Input to Bottom 1/2	9 V Swing
23. N/C	
24. V_{DDFF5} 5th Bank of Latch Drains	10
25. $\Sigma^{(+)}$ Other End of Buss Con. to Pin 6	
26. $\Sigma^{(-)}$ Other End of Buss Con. to Pin 5	
27. ΣV_{SS} Sources of Active Loads	GRD
28. ϕ_{RG} CCD Output Reset Gate Pulse	(9 V Swing, -3 V Clamp)

TABLE 2-1. TC1235 I/O PADS (cont.)

Pad Designation	Typ. Voltage
29. S_o Source of Final CCD Output Device (2 Stages)	
30. ϕ_T Buss Input Transfer Clock (Only Input)	(18 V Swing, -5.9 V Clamp)
31. ϕ_{FGR} Buss Input, Gate of Tap Reset Transistor (pulse)	(9 V Swing, 6.2 V Clamp)
32. G2 dc Gate, Input Ckt. Has Barrier Implant (Add -4 V to Measured Voltage)	4.2
33. G3 dc Gate Input Ckt.	-3.1
34. $\Sigma^{(-)}$ One End of Buss, Top Left	
35. $\Sigma^{(+)}$ One End of Buss, Top Left	
36. V_{DDFF2} 2nd Bank of Latch Drains	10
37. V_{DDFF1} 1st Bank of Latch Drains	10
38. PR_{IN1} Data Input for Top 1/2	9 V Swing
39. S_1 Monitor Port for S_1 (Low Drive Cap.)	
40. G_1 Signal Input Port, (1st Poly)	1.4 V Swing (-3.8 dc)
41. ϕ_{MOCCD} Input for ϕ_T Driver	9 V Swing
42. V_{DDCCD} 1/2 of ϕ_T Driver Output, Strobe, Predriver and Logic for ϕ_{FGR}	15
43. V_{CCCCD} 1/2 ϕ_T Driver Output	15
44. ϕ_T' ϕ_T Driver Out to Off-Chip Buffer	8 V Swing
45. ϕ_{RG} Not Used, Intended to Feed Buffer	
46. $V_{DD(\phi FGR)}$ Drain Driver Output Stage of ϕ_{FGR} Ckt.	15
47. ϕ_T' Input to Drivers for S_1 and ϕ_{FGR} (Timing)	8 V Swing
48. ϕ_{FGR} Output From Driver to Clamp	8 V Swing
49. ϕ_{ISO} Driver Output from On-Chip Load Logic	8 V Swing
50. $\phi_{\overline{LOADENABLE}}$ ISO/Reset Enable Pulse Input (Active Low)	9 V Swing
51. ϕ_{RESET} Driver Output From On-Chip Load Logic	8 V Swing
52. $V_{DDLOGIC}$ Drain Volt. Prog. Reg. Logic	10
53. ϕ_B Driver Output	8 V Swing
54. $V_{CCPRO/LOGIC}$ Output Stage Load Logic Ckt. Output Stage Prog. Reg. Dr.	10

TABLE 2-1. TC1235 I/O PADS (cont.)

Pad Designation	Typ. Voltage
55. ϕ_{PO} Osc. Input for Prog.	9 V Swing
56. ϕ_A Driver Output	8 V Swing
57. $V_{DDPRG/PRD}$ Drain Prog. Reg. Driver, Prog. Register Top 1/2	10
58. PR_{out} Data Out, Top Half	8 V Swing
59. ϕ_{ISO} Input to Top 1/2	9 V Swing
60. ϕ_{RESET} Input to Top 1/2	9 V Swing
61. V_{GGFF} Gate for the Latches	15
62. $\Sigma^{(+)}$ Other End of Buss Con. Pin 35	
63. $\Sigma^{(-)}$ Other End of Buss Con. to Pin 34	
64. ΣV_{GG} Tap FET Active Load Gate	1.3

Section 3.0

DEVICE TEST RESULTS

3.1 CORRELATION MEASUREMENTS

The autocorrelation signal for a variety of square wave and pseudo-random binary sequences were analyzed employing the test circuitry discussed in Section 2.

The linearity and symmetry of the square wave autocorrelations were good over a wide dynamic range. The device operated well at the 10-MHz transport clock frequency. For the square wave correlation shown in Fig. 3-1, the floating gates were reset once every (1024) • (100 ns) = 0.1 ms. This reset rate was employed for all the results presented.

The autocorrelation response for aperiodic maximal length pseudo-random noise (PRN) sequences was used as the major figure of merit for the correlator. The theoretical peak-to-sidelobe ratio for the PRN sequences employed was 26.5 dB. The best peak-to-sidelobe ratio attained so far with the TC1235 is 25.4 dB. The autocorrelation for one of the PRN sequences is shown in Fig. 3-2. The even symmetry about the correlation peak is easily observable. There is however a broadening of the correlation peak (two bits wide instead of one), as shown in Fig. 3-3.

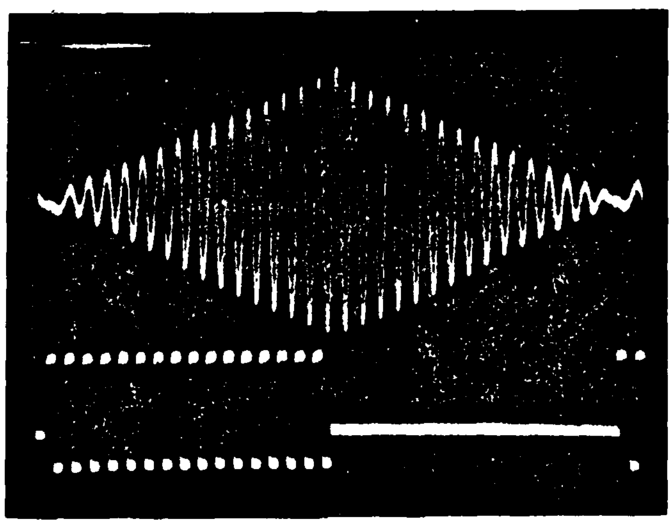


Figure 3-1. Autocorrelation of 32-bit square wave at 10 MHz (5-MHz load).

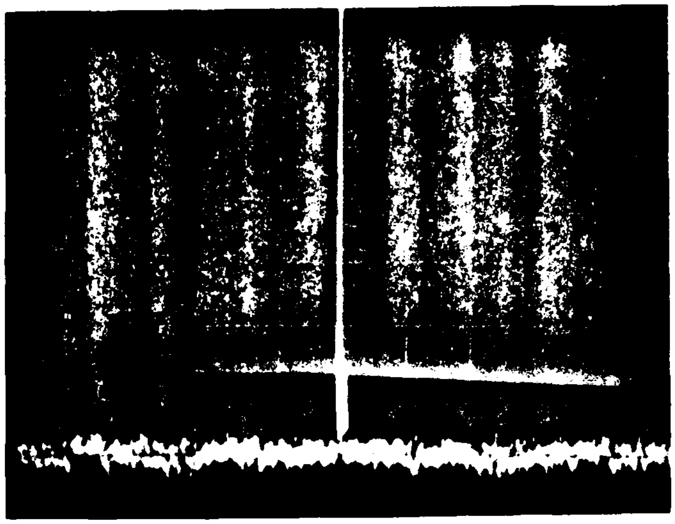


Figure 3-2. Autocorrelation for 512 PRN sequence.

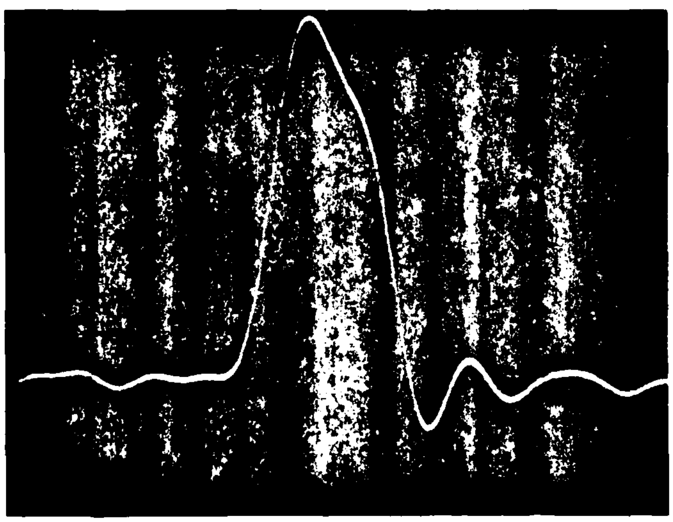


Figure 3-3. Autocorrelation for 512 PRN sequence, expanded time scale.

The broadening may be related to transfer inefficiency and the substrate modulation by the ϕ_T clock. However, a completely satisfactory explanation is not yet available. Typical results are shown in Fig. 3-4, which permits comparison between the TC1235 and an older device that had a different tap structure (TC1221).

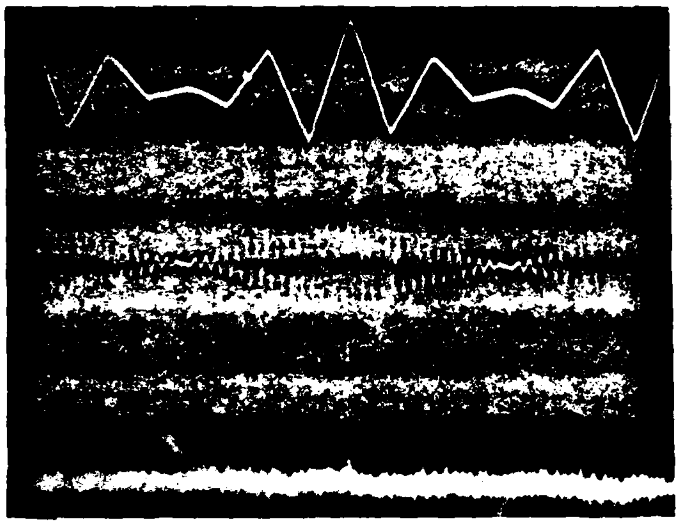
The TC1235 has a new tap structure configuration that has solved the code dependent bias problem, a term employed to describe the correlation base line change that occurs when the code is changed in the correlator reference latches and a new correlation is obtained. In earlier correlators, the device would have to be fine tuned after each code change to attain good correlation response. The code dependent bias problem is illustrated in Fig. 3-5. The device employed for this sequence of photos is the TC1221, a 128-stage CCD correlator. Photograph 1 shows the adjusted autocorrelatio. response of a square wave (10 MHz). Photograph 2 is the autocorrelator response of a PRN sequence when the device has not been adjusted from the optimal conditions employed in Photograph 2. Photograph 3 is the optimized correlation response for the PRN sequence, while photograph 4 is the autocorrelation response of the square wave with no adjustment from the conditions for photograph 3.

The correlation response (10 MHz) of the TC1235 is compared with that of the TC1221 in Fig. 3-4. For each device, no adjustment was made after the initial optimization for the square-wave response. It may be seen that the TC1221 displays the code-dependent base line shift when the code is changed from the square wave to a PRN sequence. By contrast, the photograph of the TC1235 performance shows essentially no code-dependent base line shift as the autocorrelation response changes with the code change (256-bit square wave, 32-bit square wave, 512-bit PRN code).

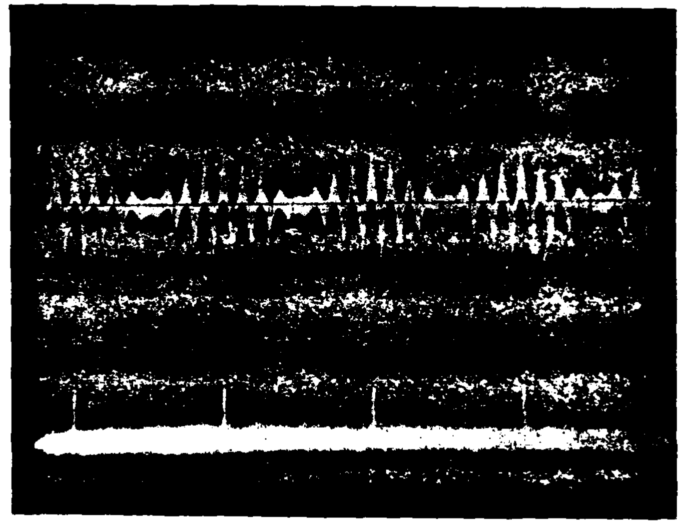
Various dynamic range measurements have been made on the TC1235, involving ratios of signal-to-clock feedthrough and signal-to-input-data feedthrough. However, all the causes of these feedthrough signals have not been determined. With further work, the feedthrough will probably be reduced. Among the changes being evaluated are improved substrate contact and rotation of the chip in the package to reduce package coupling.

The input dynamic range is 27 dB. This measurement is done by varying the CCD input signal amplitude and observing the correlation signal for a pseudorandom binary autocorrelation (at a 10-MHz clock rate). The maximum and minimum input signal levels are measured. The maximum input is defined as the point beyond which gain compression appears in the correlation output. The minimum input is defined as the point where the output correlation signal-plus-noise is equal to twice the noise.

Two output dynamic range measurements are made on the TC1235. The first is termed output signal to clock feedthrough ratio and is defined as the ratio of the maximum correlation peak amplitude to the CCD clock (ϕ_T) peak-to-peak feedthrough. The



TC1235 Performance



TC1221 Performance

Figure 3-4. Code-dependent bias results; TC1235 vs. TC1221.

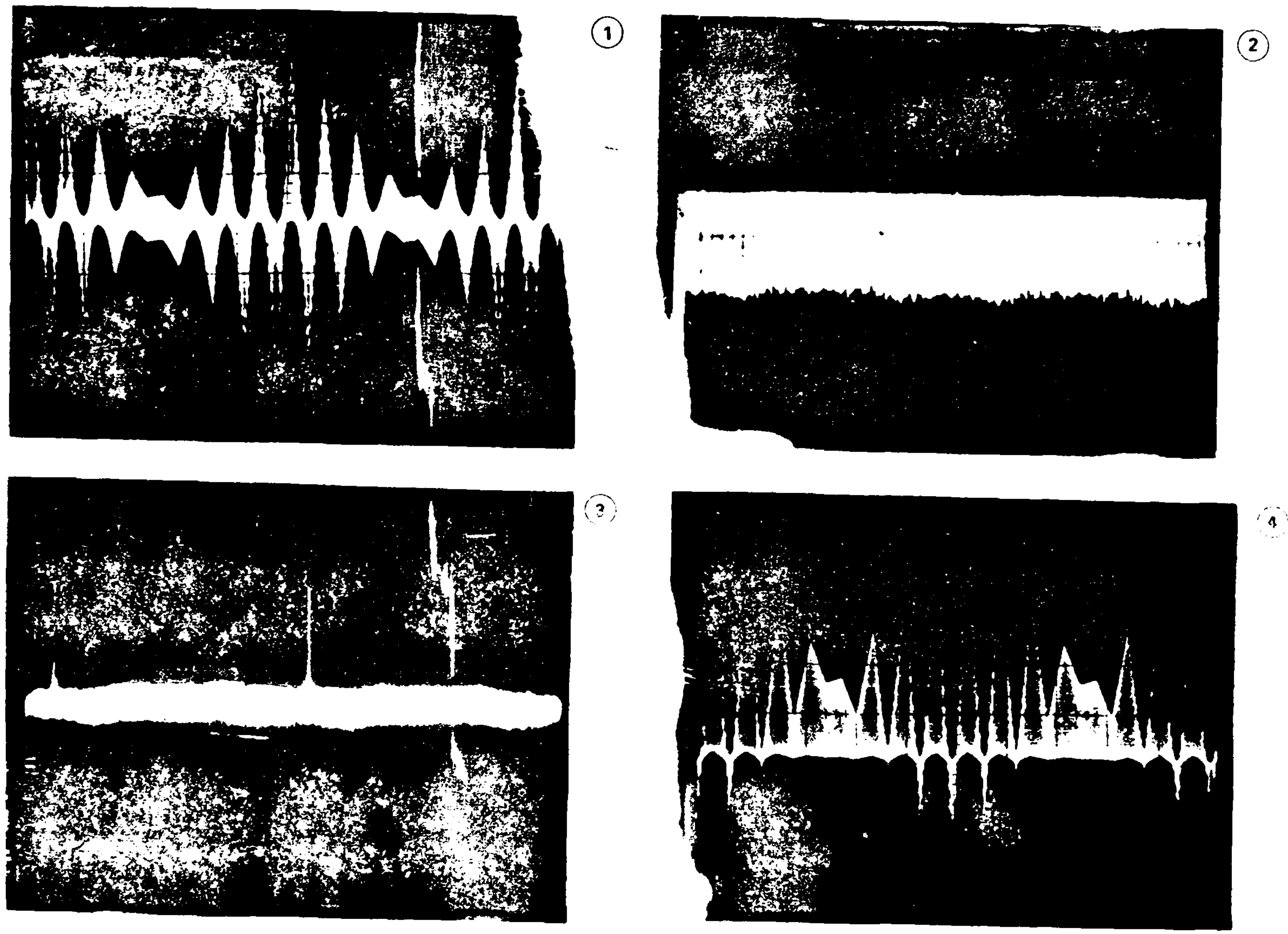


Figure 3-5. Code-dependent bias results for TC1221.

output dynamic range thus measured is 46.2 dB. The second output dynamic range is the signal-to-pattern-noise ratio. This is defined as the ratio of the maximum correlation peak amplitude to the peak-to-peak pattern noise on the clock feedthrough. The output dynamic range measured in this way is 51.6 dB.

The signal-to-noise ratio is defined as the ratio of the correlation peak amplitude to the largest peak-to-peak temporal noise of a single sample. The signal-to-noise ratio for the device is greater than 56 dB, a limit imposed by the oscilloscope used in the measurement. The "per sample" temporal noise is very small and for the foreseeable future, the dynamic range will be limited by clock feedthrough.

3.2 PROGRAM DRIVER

The program register driver produces the two clock waveforms needed to operate the program register (the reference code dynamic shift register). The input to the driver is typically a 50%-duty-cycle clock (ϕ_{PO}) of amplitude swing 0 to 5.5 V. The outputs from the driver are two complementary waveforms ϕ_A and ϕ_B, shown in Fig. 3-6. The clock ϕ_B is in phase with ϕ_{PO} and delayed by approximately 40 ns.

At the 5-MHz design rate, the program driver can successfully operate the program register, producing ϕ_A and ϕ_B clocks of 9 V amplitude. For this case of 9 V clocks (V_{DD} = 13 V, V_{CC} = 10 V), the 10% to 90% rise and fall times for the clocks are 30 ns and 25 ns, respectively.

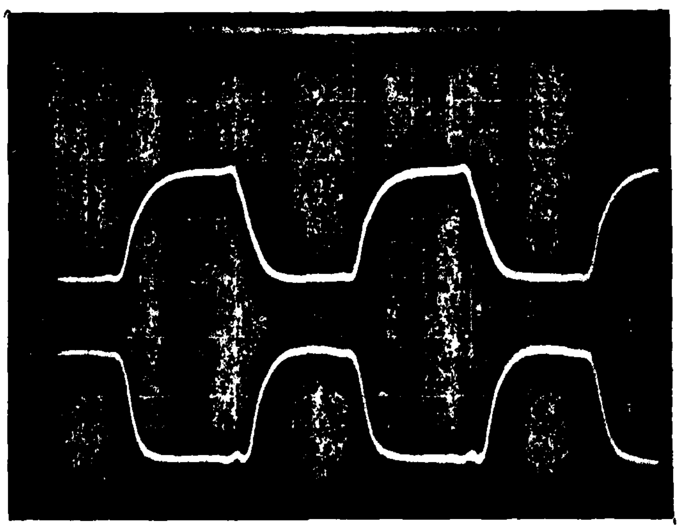


Figure 3-6. Program Register driver outputs at 5 MHz.

The driver has been operated at 10 MHz while loaded by the program register. The maximum amplitude swing at this higher frequency is 7 V.

The program driver displays a large degree of insensitivity to substrate bias. In addition, the duty cycle of the input clock (ϕ_{PO}) and therefore the output waveforms ϕ_A and ϕ_B may be adjusted over a wide range while still providing sufficient voltage swings.

3.3 PROGRAM REGISTER

The program register provides the mechanism for serially introducing the reference code into the correlator array for synchronized parallel transfer into the storage latches. The program register is divided into two 256 stage registers (top and bottom). Each of the register sections has a TTL-to-MOS-level translator at the data input and a buffer at the data output. The registers may thus be loaded in parallel, or they may be loaded in series.

The data inputs for the registers must have an amplitude swing of from 0 to 5 V (or greater). The data level at the output will swing between 0 and 11 V for V_{DD} = 13 V, and the program register clocks of 9 V amplitude.

The program register sections have been successfully cascaded and driven by the program register driver at frequencies above 10 MHz.

The program register displays a large degree of insensitivity to substrate bias and program clock duty cycle (ϕ_A and ϕ_B). However, care should be taken that the digital data entering the shift register be stable at the high or low level when the input is sampled by the ϕ_A clock. This requirement means that the data should be delayed with respect to the ϕ_{PO} clock by 60 to 120 ns (at a 5 MHz clock rate).

3.4 CCD TRANSPORT DRIVER

The CCD transport driver output synchronizes the CCD input sampling pulse (S1) the floating-gate reset pulse (ϕ_{FGR}), and the CCD transfer clock (ϕ_T). The driver supplies a properly timed pre-driver pulse to the input strobe driver and an output clock of high current drive capability (ϕ_T') for input to an external transport buffer and the floating gate reset driver.

The input to the driver is nominally a 50%-duty-cycle clock (ϕ_{MO}) of amplitude swing 0 to 5.5 V. The transport driver causes a delay of approximately 20 ns between ϕ_{MO} and ϕ_T'. The output clock has sufficient drive capability to handle a capacitive load of 130 pF with amplitude swings of 10 V* and a rise (and fall) time of 20 ns.

*(V_{DD} = 16, V_{CC} = 10)

When employing a bipolar, two stage buffer (see Par. 2.2), the driver is capable of 10-MHz operation with amplitude swings of 20 V. This performance is attained when driving the 240-pF capacitance load presented by the CCD register (which includes package capacitance). The rise time of the buffered transport clock is 20 ns, and the fall time is 30 ns when $V_{DD} = V_{CC} = 10$ V. The on-chip driver and buffer have been operated at a 20-MHz rate, fully loaded, with an output swing of 12 V.

A description of a faster buffer (that used for the correlation test results presented) is given in Par. 2.2. Typical driver waveforms are shown in Fig. 3-7.

3.5 CCD REGISTER

The CCD register is a tapped delay line employing 512 floating-gate taps. The shift register is a shallow-buried-channel, double-polysilicon-gate device. There are four gates per register stage. One pair constitutes the ϕ_T transport gates, the other gates are the second polysilicon dc-biased gate and the dc-reset floating gate. There are barrier implants under the second polysilicon gates that provide the directionality for charge transfer for each pair of gates.

The register is divided and folded between the 256th and 257th stage, creating two 256-stage registers connected by a corner diffusion. The theoretical transfer efficiency of the corner diffusion mechanism is 0.99.

Figure 3-7. Output waveforms of CCD driver at 10 MHz.

The stage length is 1.2 mils, with 0.4-mil gates and 0.1-mil overlap. The theoretical load capacitance of the ϕ_T transport gates is 210 pF. The theoretical overlap capacitance between a single floating gate and the second polysilicon transfer gates (ϕ_T) is 0.023 pF. The amount of clock coupling onto the floating gate, based on this overlap capacitance is 6% of the θ_T amplitude. The actual amount of clock coupling is significantly greater, as is explained in Appendix A.

Each of the floating gates is connected to the gate of a tap FET and to the source diffusion of a reset FET. The drain of the reset FET is connected to a common V_{BIAS} bus, which has approximately the same potential as the adjacent second polysilicon dc-biased gate (ϕ_{DC}). The gate of the reset FET is pulsed periodically to reset the floating gate to the V_{BIAS} potential. Each of the reset FETs has a channel length of 0.3 mil and a channel width of 0.4 mil. The gate is covered and periodically contacted to an aluminum drive bus (ϕ_{FGR}).

The register has a typical transfer inefficiency of $\epsilon = 1.7 \times 10^{-4}$ at a 10-MHz clock rate. The charge transfer loss per transfer was estimated from photographs such as Fig. 3-8. The amplitude of the leading "one" compared to the steady-state "one" level (or the amplitude of the first trailing "zero" as compared to the steady-state "zero" level) leads to a value of $n\epsilon = 0.17$, where n is the number of transfers and ϵ is the loss per transfer. The value of $\epsilon = 1.7 \times 10^{-4}$ is somewhat higher than

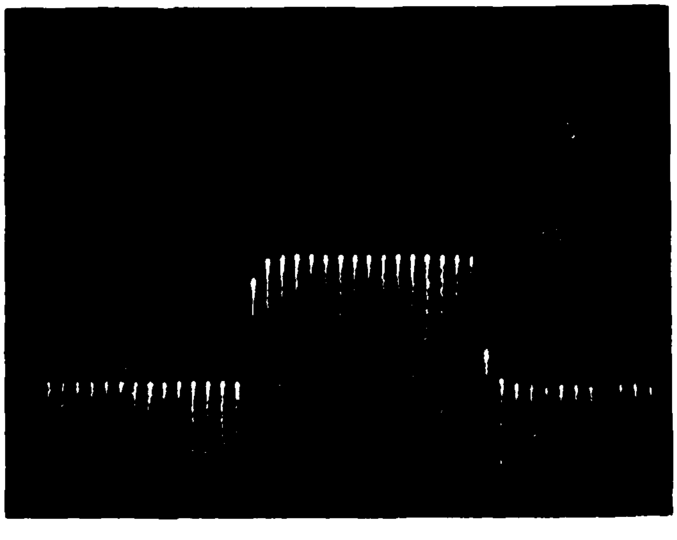


Figure 3-8. Transfer Loss at 10 MHz.

the expected value (5×10^{-5}) for the buried-channel process. This transfer loss is for the conditions of floating gate reset once every 0.1 ms and 18 V transfer clock (ϕ_T).

The effectiveness of the corner diffusion is qualitatively demonstrated in Fig. 3-9. The CCD has been driven by an impulse after a 512-bit square wave was loaded via the program register. The uniformity of the impulse response indicates that the impulse has propagated through the corner circuit with essentially no loss.

3.6 CCD INPUT

The input structure of the CCD register consists of three polysilicon gates preceded by a source-strobe diffusion. The input gates are the first polysilicon G1 and G3 gates and the second polysilicon G2 gate. The G3 gate is followed by the first gate of the first stage (a second polysilicon ϕ_T gate). There is external access to the source diffusion (S1) and the input gates. The strobe diffusion is connected on-chip to the strobe driver.

The TC1235 is designed to use the fill and spill input technique, with signal input on the G1 gate. The strobe driver produces a pulse every ϕ_T clock cycle, with appropriate amplitude swing and timing characteristics to allow narrow aperture linear sampling of the G1 input signal.

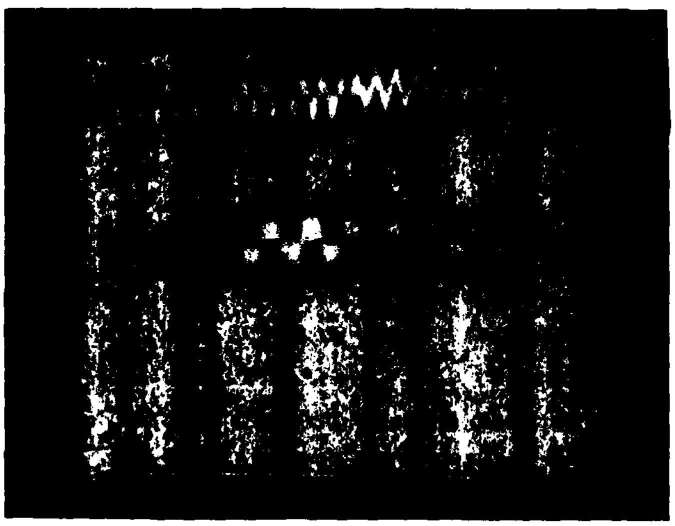


Figure 3-9. Impulse response at 10 MHz.

The strobe driver pulse has a rising edge that precedes the ϕ_T transfer clock rising edge (50% points) by nominally 12 ns (dependent upon the ϕ_T buffer). This time interval determines the charge equilibrium and sampling aperture times. The strobe driver tracks the G1 input level so that the negative-going sampling pulse (S1) will supply the input structure with charge over a wide range of G1 potential. Furthermore, the tracking capability of the strobe assures uniformity of not only sampling time but also charge supply, over the signal dynamic range.

3.7 CCD OUTPUT

The CCD register output structure consists of an isolated floating diffusion coupled to a two-stage FET output amplifier. The floating diffusion is isolated on the register side by a second polysilicon gate, which is connected to the ϕ_{DC} bus. On the reset drain side of the floating diffusion is a second polysilicon gate tied to a separate bias potential ϕ_{DC} (amp). Adjacent to the bias gate is the reset gate ϕ_{RG}, which periodically couples the floating diffusion to the reset drain (DR).

The floating diffusion is connected to the input gate of the two-stage source follower. The output of the amplifier is connected off-chip to an external load resistor (nominal value 1K). The theoretical transfer function for input charge to output voltage for this output configuration is 1.35 V per picocoulomb. The maximum expected signal voltage fluctuation at the output is 0.370 V (corresponding to a 10% to 70% full well signal swing). In actuality, the maximum observed signal voltage swing has been 0.650 V, for an estimated charge fluctuation of 15% to 95%. The discrepancy is most probably due in part to greater CCD register charge capacity than expected.

The operating potentials of the reset drain (V_{DR}), reset gate clock (ϕ_{RG}) and ϕ_{DC} (amp) are dependent upon the ϕ_{DC} and V_{BIAS} potentials. There is a requirement of significant voltage differentials between the ϕ_{DC} biased isolation gate, the ϕ_{DC} (amp) gate and reset drain. Typical biases are V_{DR} = 25 V, ϕ_{DC} (amp) = 17 V, and ϕ_{DC} = 9 V, with the ϕ_{RG} swing of -6 to +12 V (substrate at ground).

3.8 LATCHES

The reference code of the correlator is stored, during correlation periods, in the 512 latches of the latch array. The latches are four-transistor flip-flops associated with reset and load transistors. All devices are enhancement devices. The $\overline{Q}$ output is connected to a latch reset transistor and the Q output is connected via a transmission gate to a pull-down transistor, which is enabled by a stage of the program register. These nodes (Q, $\overline{Q}$) are also connected to their respective tap routing switch gates.

The latch V_{DD}, V_{GG}, and V_{SS} buses are bonded out to the package. The V_{SS} may be biased at potentials above ground to reduce power dissipation in the latch. The latches operate over a wide range of potentials for V_{DD}, V_{GG}, and V_{SS}. For a

$V_{DD} = 10$ V, $V_{GG} = 16$ V, $V_{SS} = 3.5$ V, $\phi_{RESET} = 0$ to 12 V, $\phi_{ISO} = 0$ to 12 V, and subtrate = -2 V the simulations show good latch reset and latch set times. The $\bar{Q}$ node may be reset to V_{SS} from the V_{DD} potential in 25 ns. The Q and $\bar{Q}$ nodes exhibit a rise in voltage to 95% of V_{DD} potential in 400 ns.

The complete load scenario for the latches was simulated employing the typical simulated waveforms for the program clocks and the load pulses. The total maximum time of a load cycle is 460 ns (dependent upon program data and initial conditions). This time is measured from the falling edge of the load enable pulse to the 95% of V_{DD} potential on the high output node (for the biasing conditions stated above).

Empirical evaluation has shown that the latches may be loaded successfully at clock rates in excess of the design rate of 5 MHz. Furthermore, the typical power dissipation in the latch arrays is close to the minimal 250 mW predicted by simulation.

The latch array may be selectively disabled in groups of stages 1 to 64, 65 to 128, 129 to 256, 257 to 384, and 385 to 512. This is done by taking the appropriate latch V_{DD} bus(es) to V_{SS} potential, instead of to a positive V_{DD} potential. This action causes all the routing switches associated with a turned off group to be disabled (both Σ^+ and Σ^- routing switches of a disabled stage would have gate potentials at V_{SS}).

3.9 TAP STRUCTURE

The tap structure senses the charge fluctuations under the floating gate and produces a proportional voltage fluctuation which may be contributed to one of the summation buses. A given tap's contribution is controlled by the latch-enabled routing switches (contribution to the Σ^+ bus, Σ^- bus, or no contribution). Both of the summation buses are designed to be voltage sensed and differentially summed by a circuit with high input impedance (more than 100K ohms).

The voltage on either of the summation buses will be the average of all the common node voltages of the taps connected to that bus. The On resistance of the connecting routing switches is nominally 6.4K; this is thus the impedance that couples a contributing common node to a summation bus. The output impedance of a contributing tap is nominally 16 K (impedance looking into enabled routing switch).

The quiescent current in the tap source followers (ΣV_{DD} supply) is determined primarily by the floating gate bias potential (V_{BIAS}), the active load gate bias (ΣV_{GG}), and the substrate potential. Care should be taken to keep the power dissipation in the tap structure near the design goal of 1 mW per tap. Of particular concern is that the following relationship is not violated:

$$\Sigma V_{GG} - \Sigma V_{SS} - 0.9 + 0.5 \cdot V_{sub} \leqslant 3 \text{ volts.}$$

The nominal quiescent current is 164 μA per tap for the floating-gate potential equal to 6 V, $\Sigma V_{DD} = 6$ V, $\Sigma V_{GG} = 3$ V, $\Sigma V_{SS} = 0$ V, and $V_{SUB} = -2$ V.

The linearity of the tap structure, as predicted by simulation, should be very good (THD* $\leqslant 0.5\%$). The voltage gain of the tap source follower is predicted to be

$\frac{V_{\text{common node}}}{V_{\text{floating gate}}} = 0.9$; actual measurements at 5 MHz show an ac gain of 0.89.

3.10 LOAD LOGIC

The load logic circuitry produces the signals necessary to accomplish the parallel shift of program data in the shift register to stored data in the latches. The required signals are the latch reset pulse (ϕ_{RESET}) and the program register isolation/gating pulse (ϕ_{ISO}). These signals are generated by the load logic and associated drivers in response to the load enable command ($\phi_{\overline{LOAD}}$).

The load logic sections for the generation of the reset and isolation pulses are identical; the only difference is the method of input of the program clocks ϕ_A and ϕ_B. The program clocks are input to the load logic section for the reset pulse (ϕ_{RESET}) so that the output is in phase with ϕ_A and high only when ϕ_{LOAD} is low. Similarly, the program clocks are input to the section for the isolation pulse (ϕ_{ISO}) so that the output is in phase with ϕ_B and high only when ϕ_{LOAD} is low. The design load for the reset pulse is 156 pF and the design load for the isolation pulse is 140 pF.

The load enable pulse should be 200 ns wide (for 5 MHz load) and delayed by nominally 140 ns with respect to the ϕ_{PO} program master oscillator. This timing ensures that the load enable pulse will be low (active) for a complete high period of the ϕ_A clock, followed by a complete high period of the ϕ_B clock.

The load logic dissipates a large amount of stand-by power, as detailed in the interim report. In order to shut off this circuit, to reduce the power dissipation on the chip, both the load logic V_{DD} and the V_{CC} for the load logic/program driver must be grounded. This renders both the load logic and the program driver nonoperational.

*total harmonic distortion

Section 4.0

CONCLUSIONS AND RECOMMENDATIONS

A CCD correlator chip designated TC1235 was developed on this program. Testing indicates that the device meets or exceeds most of the contractual requirements and represents a significant advance in the state of the art of signal processing with CCDs. Principal findings are summarized in the following table.

Parameter	Contract Requirement	RCA Design Goal	TC1235 Measured Performance
No. of Tapped Stages	512	512	512
CCD Clock Rate, MHz	8	10 (1)	10 (1)
Reference Code Load Rate, MHz	0.5	5 (2)	10 (2)
Dynamic Range, dB	35	45	46 (3) 51 (4)
Signal-to-noise Ratio, dB (one sample)	50	66	56 (5)
Total Transfer Loss ($n\Sigma$)	0.2	0.1	0.17
Peak-to-Sidelobe Ratio, dB (autocorrelation of 512 bit aperiodic code)		26.4 (theoretical value)	25.4

Notes:
(1) With on-chip clock driver.
(2) On-chip pre-driver and off-chip buffer.
(3) Ratio of correlation peak signal to clock feedthrough.
(4) Ratio of correlation peak signal to pattern noise on clock feedthrough.
(5) Measured on correlation waveform.

The success achieved to date with TC1235 is believed to warrant a device improvement program that would result in a more-useful and easier-to-operate device. This device improvement program would involve: (1) addition of more on-chip support circuits; (2) modification of some existing circuits; and (3) process changes leading to smaller size and better yield and performance. In category (1), the circuits of interest are: (a) automatic input biasing; (b) tap quiescent-current adjustment; (c) on-chip summing circuits. In category (2), the candidates for modification are: (a) input sampling (strobe) circuit; (b) load logic; (c) CCD output structure; (d) CCD input structure (surface channel to buried channel). Process changes in category (3) to be considered are: (a) linear reduction of all dimensions; (b) improved substrate contact; and (c) reduced overlap capacitance for CCD polysilicon gates. These modifications, along with the performance and/or yield benefits anticipated, are summarized briefly below.

Category 1: On-Chip Support Circuits

(a) Automatic Input Biasing

The current version of the TC1235 requires adjustment of the CCD shift-register input biases in order to ensure accurate sampling of the input signal and wide dynamic range. Two input gate voltages need to be adjusted for each new device in order to attain optimum operation. The proposed improvement to the current design is to incorporate a modification to the TC1235 strobe circuit and to add an automatic input biasing circuit. These improvements would make the input structure self-biasing and would greatly simplify the adjustments necessary to operate the correlator. In addition, the new ciruitry should make device interchange possible without the need to readjust CCD register potentials.

(b) Tap Quiescent Current Adjustment

The second most critical adjustment necessary for optimum correlator operation is the adjustment of the bias point for the tap structure. For linear, low-power operation of the tap circuitry, the bias potentials must be adjusted within a fairly narrow margin.

The suggested method of obviating the need for adjustment from device to device is to automatically adjust the active load-gate potential to attain the desired quiescent current for given external potentials. This could be done by employing an on-chip differential amplifier.

(c) On-Chip Summing Circuit

The correlator requires external circuitry for differential summation of the summing buses. At present, this function is performed by a video differential amplifier coupled with low-pass filtering. An attractive alternative to this method is the inclusion of an on-chip summing circuit, so that the complete correlation process will be done on-chip.

The suggested on-chip circuitry employs sample-and-hold circuitry on both summation lines followed by level-shifting inverters to shift the levels up to levels compatible with the differential amplifier. The proposed differential amplifier has five transistors with adjustable bias point for the current source. The amplifier is followed by a two- or three-stage buffer amplifier in order to drive the package capacitance and the external loading.

Category 2: Modification of Existing Circuits

Some adjustment to the design of the existing circuitry is warranted. First, the CCD input sampling strobe circuit should be slightly modified to improve the edge speed and to adjust the S1 bias point with respect to the G1 potential (S1 is designed to track G1). This is a straightforward adjustment.

A redesign of the load logic and drivers should be undertaken. This circuitry, which automatically generates the required latch loading pulses, has proved to have a lower yield than other circuits. For this reason and because the existing circuit dissipates a large amount of power in the stand-by mode, an improved version has been conceived. This version will greatly reduce the stand-by power dissipation and is slightly less complex, which should improve yield.

There are two additional areas where redesign effort may be worthwhile. The first is the floating-diffusion output-amplifier scheme for the CCD register. The linearity and dynamic range of the existing circuitry should be empirically examined and, if necessary, redesign pursued. The aim of this study would be to attain a circuit that will readily allow cascading of the TC1235 devices for longer code length capability.

The second additional area to be considered is the option to employ a surface channel input structure. This option would employ a surface channel under the G1, G2, and half of the G3 input gates. The surface channel input structure would yield a more linear voltage-to-charge conversion at the input to the CCD signal register. All the ramifications of this option should be investigated, and the impact of this technique on correlator operation evaluated.

Category 3: Process Changes

(a) Linear Reduction of all Dimensions

A reduction in device dimensions will improve yield and reduce the capacitive loading seen by the CCD driver and the program driver. This reduction in capacitance will reduce the power dissipation in the drivers and will increase the maximum clock operating frequencies. In addition, the dimensional reduction will decrease all the array parasitic capacitances at no expense in FET drive capability (W/L constant). This improvement will manifest itself in higher program register operating frequencies and faster latch resetting-setting operations.

The bandwidth of the tap structure will be increased due to the reduction of parasitic capacitance in the tap circuitry. However, the reduction in feature dimensions will affect the degree of array nonuniformity in the tap circuits. It is thought that this increase in nonuniformity due to reduction of the nominal dimensions will be tolerable for the degree of reduction proposed.

(b) Improved Substrate Contact

The TC1235 exhibits an unforeseen substrate potential modulation phenomenon. This is due to the large ϕ_T uniphase CCD transport clock combined with the method employed for setting the substrate potential. The deleterious effects inherent in this modulation phenomenon are: (1) threshold modulation (ΔV_T) due to the modulation of the body effect; (2) increased clock feedthrough; and (3) the possibility of increased nonuniformity if the first two effects are not present uniformly over the array.

The most attractive method for improving the substrate contact is the inclusion of an initial P^+ step in the current process. The addition of this step will require one additional mask and will allow direct contact to the P^- substrate via metal contacted to the P^+ diffusions.

c. Reduced Overlap Capacitance

A reduction in overlap capacitance will complement the improved substrate contact in reducing the clock feedthrough on the summation buses. The overlap may be reduced by changing the second polysilicon mask from 0.4 mil CCD gate width to 0.34 mil CCD gate width (dimension after the linear shrink and adjustment). This will reduce the mask overlap by over 30%. The mask fidelity, mask-to-mask alignment tolerance, and polysilicon etch definition tolerance are consistent with this proposed change.

APPENDIX A. SUBSTRATE POTENTIAL MODULATION

A. SUBSTRATE MODULATION

The TC1235 exhibits an unforeseen substrate potential modulation phenomenon. This is due to the large ϕ_T uniphase CCD transport clock combined with the method employed for setting the substrate potential. The devices currently employ a large N^+ diffusion ring around the periphery of the chip for contact to the P^- substrate. The N^+ ring extends into the scribe region on all sides and is contacted by metal adjacent to the substrate bond pad. This method of setting substrate potential has worked adequately on the two-phase CCD devices fabricated employing this process.

This technique depends upon the large area of the N^+ P^- junction and the lattice damage at the edges of the chip to create a 'leaky' junction of relatively low ac impedance. By this mechanism, it was thought that the substrate would be held at the dc potential of the N^+ diffusion. In actuality, the junction characteristics are such that the substrate is not held close to the dc potential applied to the substrate (N^+) bond pad. Instead, the ϕ_T clock is significantly modulating the substrate potential.

The deleterious effects inherent in this modulation phenomenon are: (1) tap circuitry threshold modulation (ΔV_T) due to the modulation of the body effect; (2) increased clock feedthrough on the summation buses; and (3) the possibility of increased nonuniformity if the first two effects are not present uniformly over the array.

B. EMPIRICAL EVALUATION AND EXPLANATION OF ϕ_T COUPLING

Empirical evaluation of ϕ_T coupling onto the summation buses has shown that as much as 31% of the ϕ_T clock amplitude is coupled onto the summation buses There are a number of reasons for the greater than expected coupling. A major reason is the substrate modulation effect.

There have been a number of methods employed to reduce the coupling due to the substrate modulation effect. All of the methods call for the reworking of the die back surface, and the application of substrate bias to the die attach in the package cavity (as opposed to relying on the bonding pad on the chip front surface for application of potential). The various processing methods employed are detailed in Table A-1. Also given in Table A-1 are test results for the amount of coupling present after processing.

It has also been found that the coupling can be reduced by approximately another 3% by rotating the chip 90 degrees in the cavity and bonding the device in a manner orthogonal to that presented in Figure 2-6.

Thus, the best (lowest) percentage of clock feedthrough presently obtainable is is on the order of 13.5%. This is the case of a back surface boron implant with a laser anneal and a 90 degree chip rotation. This figure is still about twice what was expected based on theoretical overlap capacitance calculations. The factor of two may be explained by the larger than 0.1 mil overlap between first and second polysilicon (ϕ_T gate - floating gate) and an overlap oxide of 1,900Å instead of the nominal 2,400Å. In addition, the first polysilicon to second polysilicon 'side wall' capacitance was not included in the theoretical calculations.

This explanation is consistent and quantitatively complete when compared with observed operating phenomena and processing measurements. Furthermore, the back surface processing decreases the feedthrough significantly and is a viable design correction method for the existing devices.

TABLE A-1. ϕ_T FEEDTHROUGH FOR VARIOUS PROCESSING METHODS

Processing Method	Percentage ϕ_T Feedthrough
Original parts with N^+ on back, silver conductive epoxy mounting, die attach connected.	31%
N^+ etched off back, chrome-gold metallization, gold-tin solder mounting, die attach connected.	17.2%
N^+ etched off back, boron implant, low temperature anneal, chrome-gold metallization, silver conductive epoxy mounting, due attache connected.	Not Available
N^+ etched off back, boron implant, laser anneal, chrome-gold metallization, gold-tin solder mounting, die attach connected.	16.5%

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